Applying Cost Engineering for cost effective design engineering

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It’s hard to imagine a world without chips
Everyday objects get connected

GPS Fleet tracking

Smart meters

Wireless IP camera

Cash registers
New devices, new applications

- Wearable sensors (Holst Centre)
- Micromirrors for beamers (TI)
- Accelerometer (IC Mechanics)
- Camera pill with camera, transmitter and computer
- DNA analysis (Affymetrix)
- Gyroscope (UC Irvine)
- On-Chip DNA amplification and detection (imec/Panasonic)
- Lab on a Chip (LOC) for counting red blood cells
A virtuous cycle
More than 200 billion ICs are made every year

In 2013, 202 billion ICs were produced — 28 for every man, woman and child on the planet.

Global semiconductor industry sales were $305.6 billion.

Data: WSTS
ASML makes the machines for making those chips

- Lithography is the critical tool for producing chips
- All of the world’s top chip makers are our customers
- 2013 sales: €5.2 bln
- Payroll: ~13,800 FTEs
Gordon Moore (1965): Number of transistors per chip doubles every year.

Later adjusted to two years, the trend has held for more than four decades.
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Later adjusted to two years, the trend has held for more than four decades.
Moore’s Law makes chips cheaper…

Source: Gartner. High quality Flash
Keeping up with Moore’s Law

PAS 2000
ASML’s first stepper, 1984

TWINS SCAN NXT:1970Ci
The most advanced immersion scanner, 2013
The future of lithography: EUV

- Large vacuum chamber
- New light source
- Mirror optics
Open Innovation from design to manufacturing

- Customers
  - Semiconductor producers

- Co-solution network
  - Mask, Resist, Wafer track
  - Wafer processing

- Supplier and partner network
  - Optics, measurement systems, parts, subsystems

- Virtual innovation network
  - Academia, technology providers, research institutes
Sharing risk and reward

Suppliers bear some of the risk and participate in the rewards.

Mutual transparency ensures that risks are well understood and minimized.

“QLTC” sourcing model (Quality, Logistics, Technology, Cost) means that suppliers do not compete solely on cost.
Why is cost important: The Business drivers

- Customers will only increase investments in lithography if we prove that we can help them continue Moore’s Law towards smaller, more powerful and energy-efficient chips at similar cost.

- Consistent strategy: there are challenges to reaching our goals. Cost is the biggest one; so affordability is key.

- Mobile applications are leading innovation. Our challenge is affordable scaling that creates lower cost and improved performance – possible with both EUV and immersion technology.
Create Cost transparency through the CE Cost Calculation bucketing

CoG Roadmap

Bucketing the Gap

Need more transparency

ASML Business Norms
Technical Costs

1. Identify solutions incl Manufacturing & Supplier ideas
   Decision support on cost impact

2. Sup. Validation
   MRO
   LBR Rates
   MFG Rates
   Preferred Suppliers
   MFG + LBR Processes
   SG&A
   Finance
   R&D
   Profit
   MFG Set Up
   MFG CT
   Labor
   LRO

Actual Supplier Costs
Volume Price Supplier Roadmap
CE Product Cost Calc.
Design CoG Spec.
Areas in PGP where CoG is managed

Cost of Goods spec organized as any other performance spec

PGP: Product Generation Process
The Design Project Leader organizes the CoG team assignment to meet design & best cost

CoG as part of the industrialization fundamentals during design engineering

- **Architects:** Functional CoG spec [EPS], cascading to functional clusters and building blocks
- **Designer engineers:** [DfX] Design for manufacturability & design cost estimations
- **Value Engineers:** Design to Cost, identify solutions for integral cost optimizations with focus on Product incl Manufacturing & Supplier ideas
- **Cost Engineers:** Decision support on CoG Support Technical Costs, Validation @ Suppliers
- **Buyers:** Cost down roadmap Suppliers
- **Supply Chain Engineers:** New Product Introduction, Technical Acceptance by Suppliers [Learning Curve, NRE, Tooling costs]
- **Logistic Engineers:** Cycle time & cost reduction throughout the Supply Chain
Typical Cost Engineering support & deliverables

- Building and maintain CoG Monitors
- Product Cost calculations
- Publishing product cost data in CoG tooling used by designers
- Design decision support on CoG
- Technical Cost Validation by Suppliers
- Sourcing support during negotiations @ Suppliers
- Feedback for designer engineers [guidance & rules]
The Cost Engineering competences

### COST ENGINEERING COMPETENCES

**Detailed description of the different industrial manufacturing technologies and manufacturing processes:**

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Visit our [Cost Engineering Competences](#)
Typical Cost Engineering feedback to designers:
Why functional design is not enough
Example: simple design

Function: a block needs to be placed in a corner.
Integral cost price part < 30 euro.
Cycle time part < 2 days
Is this a good design?

Design nr. 1

- Sharp corner
- Small chamfer is required to meet function.

Function OK!
Block can be placed in corner

Production

Can be made!!

- Step 1 milling
- Step 2 EDM

Result

- Function **OK**
- Integral cost price **100 euro**
- Cycle time **5 days**
Is this a better design?

**Design nr. 2**

- Small radius
- Block can be placed in corner

**Function**
- Relatively large chamfer is required to meet function.
  - Function OK!

**Production**
- Can be made!!
  - Step 1 milling
  - Step 2 milling corner

**Result**
- Function OK
- Integral cost price **35 euro**
- Cycle time **2 days**
Is this the best design?

Design nr. 3

Function:
- Chamfer not required for function
- Function OK!
- Block can be placed in corner

Production:
- Can be made!!
- Step 1 milling

Result:
- Function OK
- Integral cost price 20 euro
- Cycle time 1 day
Why design for manufacturability + cost?

Design for manufacturability is not a goal, but a method to reduce:

- 100 euro
- 5 days
- 65 euro
- 3 days
- 80 euro
- 4 days

Design nr. 1

Design nr. 2 vs. nr. 1

Design nr. 3 vs. nr. 1
Cost Engineering competence provides Manufacturing Process Knowledge

Sample design rules……

**General:**
- Cost/part is driven by Geometric dimensioning and tolerancing & roughness spec.

**Machining:**
- Avoid thin walls
- Minimize number of tools required
- Avoid features deeper than 5 * D
- Avoid exotic materials (Ti, Inconel, PEEK)

**Sheet Metal:**
- Combine as much as possible bends into one part piece
- Bending radius ≥ Material thickness

**Additive Manufacturing**
- Combine as little as possible part volume with as little as possible building height.
Thank You