

# Applying Cost Engineering for cost effective design engineering

**Ronald Provoost** 

Sr Manager Cost Engineering

Nov 2014

# It's hard to imagine a world without chips















# Everyday objects get connected



**ASML** 

Smart meters

camera

# New devices, new applications

## **ASML**



Wearable sensors (Holst Centre)



Camera pill with camera, transmitter and computer



DNA analysis (Affymetrix)



Gyroscope (UC Irvine)



Accelerometer (IC Mechanics)



Micromirrors for beamers (TI)



On-Chip DNA amplification and detection (imec/Panasonic)



Lab on a Chip (LOC) for counting red blood cells



# More than 200 billion ICs are made every year



IC units, in billions

In 2013, 202 billion ICs were produced — 28 for every man, woman and child on the planet. ASML

Global semiconductor industry sales were \$305.6 billion.

# ASML makes the machines for making those chips



• Lithography is the critical tool for producing chips

- All of the world's top chip makers are our customers
- 2013 sales: €5.2 bln
- Payroll: ~13,800 FTEs

# Driving the semiconductor industry: Moore's Law



Gordon Moore (1965): Number of transistors per chip doubles every year. ASML

Later adjusted to two years, the trend has held for more than four decades.

# Driving the semiconductor industry: Moore's Law

#### Microprocessor Transistor Counts 1971-2011 & Moore's Law



Gordon Moore (1965): Number of transistors per chip doubles every year. ASML

Later adjusted to two years, the trend has held for more than four decades.

# Moore's Law makes chips cheaper...



# Keeping up with Moore's Law







PAS 2000 ASML's first stepper, 1984 TWINSCAN NXT:1970Ci The most advanced immersion scanner, 2013

# The future of lithography: EUV



# Open Innovation from design to manufacturing

## ASML

Customers Semiconductor producers

Co-solution network Mask, Resist, Wafer track Wafer processing



Supplier and partner network Optics, measurement systems, parts, subsystems

Virtual innovation network Academia, technology providers, research institutes

# Sharing risk and reward

## ASML



Suppliers bear some of the risk and participate in the rewards.

Mutual transparency ensures that risks are well understood and minimized.

"QLTC" sourcing model (Quality, Logistics, Technology, Cost) means that suppliers do not compete solely on cost.

# Why is cost important: The Business drivers

- Customers will only increase investments in lithography if we prove that we can help them continue Moore's Law towards smaller, more powerful and energy-efficient chips at similar cost.
- Consistent strategy: there are challenges to reaching our goals. Cost is the biggest one; so affordability is key.
- Mobile applications are leading innovation. Our challenge is affordable scaling that creates lower cost and improved performance – possible with both EUV and immersion technology.

## Create Cost transparency through the CE Cost Calculation bucketing Bucketing the Gap Need more transparency



# Areas in PGP where CoG is managed



Cost of Goods spec organized as any other performance spec



PGP: Product Generation Process

The Design Project Leader organizes the CoG team assignment to meet design & best cost

CoG as part of the industrialization fundamentals during design engineering

ASML

Architects: Functional CoG spec [EPS], cascading to functional clusters and building blocks Designer engineers: [DfX] Design for manufacturability & design cost estimations > Value Engineers: Design to Cost, identify solutions for integral cost optimizations with focus on Product incl Manufacturing & Supplier ideas Cost Engineers: Decision support on CoG Support Technical Costs,  $\geq$ Validation @ Suppliers Cost down roadmap Suppliers > Buyers: Supply Chain Engineers: New Product Introduction, Technical Acceptance by Suppliers [Learning Curve, NRE, Tooling costs] Cycle time & cost reduction throughout the Supply Logistic Engineers: Chain



# Typical Cost Engineering support & deliverables

- Building and maintain CoG Monitors
- Product Cost calculations
- > Publishing product cost data in CoG tooling used by designers
- Design decision support on CoG
- Technical Cost Validation by Suppliers
- Sourcing support during negotiations @ Suppliers
- Feedback for designer engineers [guidance & rules]

### **ASML**

# The Cost Engineering competences

#### COST ENGINEERING COMPETENCES

Detailed description of the different industrial manufacturing technologies and manufacturing processes:	
Knowledge Sharing	CE - Electronics Manufacturing + Cost competence
Process Description	SMT Manufacturing
<ul> <li>ASML experts &amp; Supplier experts feed back</li> </ul>	Coating
Area of application	Manual Assembly
Industrial equipment	
Industrial Norms	
Best practices& Design Rules	
Cost Driver information	
CE - Mechanics Manufacturing + Cost competence	CE - Optics Manufacturing + Cost competence
• Machining	CNC Optical Machining
Welding & Brazing	• Litho
Sheet Metal & Forming	Grinindg Polishing
Heat & Surface treatments	Measuring & Inspection
Cleaning	Coating
Specials	Specials
Visit our <u>Cost Engineering Competences</u>	

Typical Cost Engineering feedback to designers: Why functional design is not enough Example : simple design

ASML



Function: a block needs to be placed in a corner. Integral cost price part < 30 euro. Cycle time part < 2 days

# Is this a good design?



## Production

Can be made!!

Step 1 milling



#### Step 2 EDM



ASML

#### Function **OK**

Integral cost price 

**100 euro** 

Cycle time **5 days** 

# Is this a better design?



## Block can be placed in corner

## Production

Can be made!!

Step 1 milling

Result



#### Step 2 milling corner

ASML



# Function OK

• Integral cost price

<u>35 euro</u>

Cycle time <u>2 days</u>



# Why design for manufacturability + cost ?

Design for manufacturability is not a goal,

but a method to reduce: and





Cost Engineering competence provides Manufacturing Process Knowledge

## Sample design rules.....

#### General:

• Cost/part is driven by Geometric dimensioning and tolerancing & roughness spec.

#### Machining:

- Avoid thin walls
- Minimize number of tools required
- Avoid features deeper than 5 \* D
- Avoid exotic materials (Ti, Inconel, PEEK)

#### **Sheet Metal:**

- Combine as much as possible bends into one part piece
- Bending radius ≥ Material thickness

#### Additive Manufacturing

• Combine as little as possible part volume with as little as possible building height.

- Process description
- ASML CE expertize
- Area of application
- Industrial equipment
- Industrial norms
- Best practices
- Design rules
- Cost driver
   information

**ASML** 

# Thank You